Microprocessor and Interfacing (EE-309F)

Aptitude Questions

1. What are machine language and assembly language programs?

   The software developed using 1's and 0's are called machine language programs.
   The software developed using mnemonics are called assembly language programs.

   2. Why data bus is bi-directional?

   The microprocessor has to fetch (read) the data from memory or input device for processing and after processing, it has to store (write) the data to memory or output device. Hence the data bus in microprocessor is bi-directional.

   3. Why interfacing is needed for I/0 devices?

   Generally I/O devices are slow devices. Therefore the speed of I/O devices does not match with the speed of microprocessor. Therefore, an interface is provided between microprocessor and I/O devices.

   4. What is data size in a microprocessor?

   The Data size is the size of the operand that can be processed by an ALU in a microprocessor.

   5. Why EPROM is mapped at the beginning of memory space in 8085 system?

   In 8085 microprocessor, after a reset, the program counter will have the address 0000H. The monitor program is a permanent program for Initialization and configuring of peripherals and it is stored in the EPROM memory. If EPROM memory is mapped at the beginning of memory space, i.e., at 0000H, then the monitor program will be executed automatically after a reset of the processor. This is why EPROM is mapped at the beginning of memory space.

   6. What is Tri-state logic?

   A device can reside in three states, which are a) On-state b) Off-state and c) High impedance-state. The high impedance state is a state in which the output of a device is physically connected to a bus, but electrically isolated through high impedance.

   7. Define Stack and Stack Pointer.

   Stack is a portion of RAM memory which is used for temporary storage of register contents using PUSH and POP instructions. Stack Pointer (SP) is a 16-bit register that holds the memory address of the stack top. Stack pointer gets decremented by 2, for every push operation and vice versa.

   8. Define Program Counter.

   Program Counter (PC) is a 16-bit register which holds the memory address of the instruction to be executed next. Program counter gets incremented by 1 for every execution of the instruction.

   9. What is the significance of IO/M pin?

IO/M pin is an I/O or Memory access indicator. It asserts to high level (1), when the processor access the I/O device and it goes to low level (0), when the processor access the memory for read/write operations.

10. State the function of HOLD and HLDA pins in 8085.

The HOLD and HLDA pins in 8085 are used in interfacing the 8257-DMA controller IC with the processor.
A signal is sent by 8257 to HOLD pin in µP, to request the µP to stop its current process and allocate the buses for DMA data transfer.
µP acknowledges the request for DMA data transfer by 8257, by sending a signal in HLDA to 8257.

11. State the significance of X1 and X2 pins of 8085.

The clock signal is supplied to the microprocessor 8085 by connecting either LC, RC or quartz crystal across the pins X1 and X2. Out of the three, quartz crystal is preferred because of its high stability.

12. What is an Interrupt? How the interrupts are classified?

Interrupt is a signal send by an external device to the processor (or special instruction executed in a program), to stop the execution of the current process in the microprocessor and perform a particular task (ie., data transfer) between the processor and the called device.
They are three methods of classifying interrupts.
Method I : The interrupts are classified into Hardware and Software interrupts
Method II : The interrupts are classified into Vectored and Non-Vectored interrupts.
Method III : The interrupts are classified as Maskable and Non-maskable interrupts.

13. Distinguish I/O mapped I/O and memory mapped I/O.

Mapping is the process by which the addresses are allocated to the I/O devices.
The two kinds of mapping are a) Memory mapped I/O
b) I/O mapped I/O

Memory mapped I/O	Standard I/O mapped I/O
1. 16-bit address is allotted to each I/O device.	1. 8-bit address is allotted to each I/O device.
2. The I/O devices are accessed by Memory Read or Memory Write machine cycles.	2. The I/O devices are accessed by I/O Read or I/O write machine cycles
3. All instructions related to memory can be used to access I/O devices.	3. Only IN and OUT instructions can be used to access I/O devices.
4. Large number of I/O devices can be interfaced.	4. Only small number of I/O devices can be interfaced.
5. Data transfer can be made between all registers and I/O devices.	5. Data transfer can be made only

between Accumulator and I/O
devices.
6. This scheme is used when memory
requirement is less.
6. This scheme is used when complete
memory space is required.

14. Explain the concept of demultiplexing AD0-7 lines in 8085?

Demultiplexing is the process of separating the low byte Address (A0-7) and Data (D0-7) from the multiplexed lines AD0-7 lines of 8085, using a latch and Address latch enable (ALE) signal.
When low byte address (A0-7) comes out of AD0-7 lines, the processor asserts HIGH in the ALE pin, enabling the latch to separate the low byte address.

15. What is memory mapping?

The memory mapping is the process of interfacing memories to microprocessor and allocating addresses to each memory locations.

16. Explain the execution of the instruction CMA instruction in 8085.

CMA instruction is used to perform 1's complement of the contents of Accumulator in 8085.

17. What is the function performed by SIM and RIM instruction.

SIM Instruction:
The SIM instruction is used to mask the hardware interrupts RST7.5, RST6.5 and RST5.5. It is also used to send data through SOD line.
RIM Instruction:
The RIM instruction is used to check whether an interrupt (RST7.5, RST6.5 and RST5.5) is masked or not. It is also used to read data from SID line.

18. What will be the outcome, in execution of instructions LXI H, 4600H and LHLD 4600H?

When LXI H,4600 is executed, the number 4600 will be loaded into HL register pair.
When LHLD 4600 is executed, the contents of memory location 4600H and 4601H will be transferred into HL register pair.

19. Explain the function of IN and OUT instructions.

Execution of an IN instruction will transfer one byte of data from an Input device to Accumulator of microprocessor.
Execution of an OUT instruction will transfer one byte of data from Accumulator of microprocessor to an Output device.

20. Compare System bus and CPU bus.

Bus is a set of conducting wires in a microprocessor based system, which helps to carry various information like DATA, ADDRESS and CONTROL signals.
Bus Internal External CPU bus System Bus System Bus CPU Bus It will not be directly connected to CPU It will be directly connected to CPU There will be separate data,
address & control buses The data and address may be multiplexed

21. List the various interrupts in 8085.

HARDWARE interrupts: TRAP, RST7.5, RST6.5, RST5.5, INTR (5 Nos)
SOFTWARE interrupts: RST0, RST1, RST2, …… RST7 (8 Nos)

22. What is meant by Vectored and Non-Vectored interrupt?

When an interrupt is accepted, if the processor control branches to a specific address defined by the manufacturer then the interrupt is called vectored interrupt. All interrupts except INTR are vectored interrupts.
In Non-vectored interrupt there is no specific address for storing the interrupt service routine. Hence the interrupted device should give the address of the interrupt service routine. INTR is a non-vectored interrupt.

23. When the 8085 processor accept hardware interrupt?

The processor keeps on checking the interrupt pins at the second T -state of last Machine cycle of every instruction.
If the processor finds a valid interrupt signal and if the interrupt is unmasked and enabled then the processor accepts the interrupt. The acceptance of the interrupt is acknowledged by sending an INTA signal to the interrupted device.

24. What is masking and why it is required?

Masking is preventing the interrupt from disturbing the current program execution. When the processor is performing an important job (process) and if the process should not be interrupted then all the interrupts should be masked or disabled.
In processor with multiple 'interrupts, the lower priority interrupt can be masked so as to prevent it from interrupting, the execution of interrupt service routine of higher priority interrupt.

25. When the 8085 processor will disable the interrupt system?

The interrupts of 8085 except TRAP are disabled after anyone of the following operations
1. Executing EI instruction.
2. System or Processor reset.
3. After acceptance of an interrupt.

26. Define T-State.

A T-State is the time period of the one complete cycle of the internal clock signal of the processor. The time taken to execute a machine cycle is expressed in terms of T-states.
In 8085, if the external clock frequency applied through X1 & X2 pins are 6 MHz; then the internal clock frequency is 3 MHz (since, Fint = Fext / 2).Therefore, one T-State equals to T = 1/F = 1/3MHz = 0.333μs.

27. What is Processor (machine) cycle? List the various machine cycles with its T-states.

The machine cycles are the basic operations performed by the processor, while instructions are executed. The time taken for performing each machine cycle is expressed in terms of Tstates.
The various machine cycles are
1. Opcode fetch …….. - 4 / 6 T
2. Memory Read ……. - 3 T
3. Memory Write …… - 3 T
4. I/O Read …….. - 3 T
5. I/O Write ……. - 3 T
6. Interrupt Acknowledge …… - 6 / 12 T
7. Bus Idle …… - 2 / 3 T

28. What is the need for timing diagram?

The timing diagram provides information regarding the status of various signals, when a machine cycle is executed. The knowledge of timing diagram is essential for system designer to select matched peripheral devices like memories, latches, ports, etc., to form a microprocessor system.

29. Write an assembly language program to store the contents of the flag register in memory location 2000H.

PUSH PSW - Stores the contents of Accumulator & Flag register in Stack
POP D - Restores the stored contents of stack to DE register pair
MOV A, E - Move the contents of E register to Accumulator
STA 2000H - Contents of Accumulator is now stored to memory location 2000H
HLT

30. List the various addressing modes in 8085 with two examples in each.

Addressing is the method of specifying the location of data in an instruction.
The different types of addressing modes in 8085 are
a) Direct:
The data is stored in memory and 16 bit address of data in memory location is specified in the instruction. Eg.: LDA 4500, LHLD 4200
b) Immediate:
The required data for processing is given next to the Opcode, in the instruction itself.
Eg.: MVI A, 55 CPI 64, ADI 0A
c) Register:
The data is placed in a register and the register name is given in the instruction to access the data. Eg.: MOV A,B ADD B, SUB C
d) Register Indirect:
The data is stored in memory and the 16-bit address of the data location in memory is placed in a register pair. This register pair holding the 16-bit address is given in the instruction to access the data. Eg.: LXI, H 4250 MOV A, M
e) Implied:
The data location & the operation to be performed is given in the instruction itself.
Eg.: CMA, RAR, XCHG

31. Compare CALL and JMP instructions.

CALL Instruction:
Execution of a CALL instruction will transfer the program control from existing program to another program. ie., Sub program specified by the 16-bit address in CALL instruction will be executed. The called program should have RET – return instruction as its last instruction.
Time taken for its execution is 9 / 18 T.
Main _____ addr16:_____
_____ _____
_____ _____
_____
CALL addr16 _____
_____ _____
_____
_____ RET

JMP Instruction
Execution of a JMP instruction will transfer the program control from one location to

another location within the same program. Time taken for its execution is 7 / 10 T
Main _____
_____
_____
JMP addr16
_____
_____
addr16:_____
_____

32. Write an ALP for time delay using a register pair available in 8085.

Main _____ Delay: LXI D, Data16
_____ loop: NOP …….. 4T
_____ NOP …….. 4T
NOP …….. 4T
CALL Delay DCX D …….. 6T
_____ JNZ loop …….. 10T
_____ RET

The register pair used is DE. 28T
The total time delay made is as follows.
One T-state = 1 / Finternal
Total T-States for delay = Delay time (in μs) / Time period for 1 T-state
T–states (in execution of loop – one time) = 4T + 4T + 4T + 6T + 10T = 28T
\Data16 = Total T-States in delay program / 28T

33. Explain the Instruction format of 8085.

The 8085 have 74 basic instructions. The
size of 8085 instructions can be either 1 byte,
2 bytes or 3bytes.
1 Byte instruction has Opcode alone.
2 Bytes instructions have 1 byte
Opcode followed by 8 bit data.
3 Bytes instruction have 1 byte
Opcode followed by 16 bit data.

34. Draw and label the flags in flag register of 8085.

35. Draw the flow chart of a counter.

The counter is an arrangement to keep track of a process. This consists of three operations which are a) count initialization b) decrement count value and c) check whether count value has reached zero.
The count operation can be either Up-count or Down-count. A Counter is used for repeated processing, time delay generation, counting of events.

36. Write an 8085 program to generate a time delay of 0.4sec; assuming crystal frequency as 5MHz.

Internal frequency = 5MHz/2 = 2.5MHZ.
Time for one T-state = 1/ 2.5MHz = 0.4msec.
Number of T-states required for delay = Delay time / Time for 1T-state

= 0.4sec / 0.4msec
= 1 x 106 T-states
Delay program:
LXI B, Count …….…… 10T
Loop : MOV A, C ……..... 4T
ORA B ……..… 4T
DCX B ……..…… 6T
JNZ Loop ……..… 10T
Total T-states needed = 10T + (Count*24T)
1 x 106 = 10 + (Count x 24)
\Count = (1000000 – 10) / 24 = 41666.25D @ 41666D = A2C2H.

37. Identify the no. of address lines needed for interfacing 8KB memory.

Where, N is number of address lines. \The no. of address lines for 8 KB is equal to 13.

38. Why address bus is unidirectional?

The address is an identification number used by the microprocessor to identify or access a memory location or I / O device. It is an output signal from the processor. Hence the address bus is unidirectional.

39. How the microprocessor is synchronized with peripherals?

The timing and control unit synchronizes all the microprocessor operations with clock and generates control signals necessary for communication between the microprocessor and peripherals.

40 What is a programmable peripheral device?

If the functions performed by a peripheral device can be altered or changed by a program instruction then the peripheral device is called programmable device. Usually the programmable devices will have control registers. The device can be programmed by sending control word in the prescribed format to the control register.

41. What is the need for a Port?

The I/O devices are generally slow devices and their timing characteristics do not match with processor timings. Hence the I/O devices are connected to system bus through the ports.

42. What is handshake port?

Explain the working of a handshake input port and output port.
In handshake port, signals are exchanged between I/O device and port or between port and processor for checking or informing various condition of the device.
In handshake input operation, the input device will check whether the port is empty or not. If the port is empty, then the data is loaded into the port. When the port receives the data, it will inform the processor for read operation. Once the data have been read by the processor, the port will signal the input device that it is empty. Now the input device can load another data to port and the above process is repeated.
In handshake output operation, the processor will load a data to port. When the port receives the data, it will inform the output device to collect the data. Once the output device accepts the data, the port will inform the processor that it is empty. Now the processor can load another data to port and the above process is repeated.

43. What are the internal devices of 8255?

The internal devices of 8255 are port-A, port-B, port-C and Control register.
The ports can be programmed for either input or output function in different operating modes.

44. What are the operating modes of port -A 8255?

The port-A of 8255 can be programmed to work in anyone of the following operating modes as input or output port.
Mode-0 : Simple 1/0 port.
Mode-I : Handshake 1/0 port
Mode-2 : Bidirectional 1/0 port

46. What are the functions performed by port-C of 8255?

1. The port-C pins are used for handshake signals.
2. Port-C can be used as an 8-bit parallel 1/0 port in mode-0.
3. It can be used as two numbers of 4-bit parallel port in mode-0.
4. The individual pins of port-C can be set or reset for various control applications.
7. Draw the control word format for I/O mode.
8. Draw the control word format for BSR (Bit Set Reset) Mode.

8251 – USART:

49. What is baud rate?

The baud rate is the rate at which the serial data is transmitted (expressed as bits per second). Baud rate is also defined as l/(Tb - time period for a symbol). In some systems, one data bit may be represented through one symbol. Then, on such occasions, the baud rate and bits/sec are same.

50. What is USART? What are the functions performed by INTEL 8251A?

The device which can be programmed to perform Synchronous or Asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter).
The INTEL 8251A is an example of USART.
The INTEL 825lA is used for serial data transmission or reception either asynchronously or synchronously. The 8251A can be used to interface MODEM for serial communication through telephone lines.

51. What is asynchronous data transfer scheme?

In asynchronous data transfer scheme, first the processor sends a request to the device for read/write operation. Then the processor keeps on polling the status of the device. Once the device is ready, the processor executes a data transfer instruction to complete the process.
The frame format in Asynchronous data transfer is given below.
Start
Bit
Data (8-bits)
Parity
Bit
5top
Bit(s)
Direction of Data Transfer

52. What is synchronous data transfer scheme?

For synchronous data transfer scheme, the processor does not check the readiness of the device after a command has been issued for read/write operation. In this scheme, the processor will request the device to get ready and then read/write to the device immediately after the request. In some synchronous schemes a small delay is allowed after the request.
Data is sent continuously in blocks either without any time interval or in fixed time intervals.

53. What are the control words of 8251A and what are its functions?

The control words of 8251A are Mode word and Command word. The mode word informs 8251 about the baud rate, character length, parity and stop bits. The command word can be send to enable the data transmission and reception.

54. What are the functions performed by INTEL 8251A?

The INTEL 825lA is used for converting parallel data to serial or vice versa. The data transmission or reception can be either asynchronously or synchronously. The 8251A can be used to interface MODEM and establish serial communication through MODEM over telephone lines.

55. What is the information that can be obtained from the status word of 8251?

The status word can be read by the CPU to check the readiness of the transmitter or receiver and to check the character synchronization in synchronous reception. It also provides information regarding various errors in the data received. The various error conditions that can be checked from the status word are parity error, overrun error and framing error.

56. What are the different types of errors that can occur in asynchronous serial communication?

1. Framming Error
2. Over run Error
3. Parity Error

57. What is the significance of C/D signal in 8251?

This pin is used to select either Control register for configuring or Data bus buffer for read / write operations.
8279 – KEYBOARD & DISPLAY CONTROLLER:

58. What are the different scan modes of 8279?

The different scan modes of 8279 are Decoded scan and Encoded scan.
In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.
In encoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output.

59. What is debouncing?

When a key is pressed, it bounces after a short time. If a key code is generated immediately after sensing a key actuation, then the processor will generate the same keycode a number of times. (A key typically bounces for 10 to 20 msec). Hence the processor has to wait for the key bounces to settle before reading the keycode. This process is called keyboard debouncing.

60. What is the difference in programming the 8279 for encoded scan and decoded scan?

If the 8279 is programmed for decoded scan then the output of scan lines will be decoded output and if it is programmed for, encoded scan then the output of scan lines will be binary count. In encoded mode, an external decoder should be used to decode the scan lines.

61. What is scanning in keyboard and what is scan time?

The process of sending a zero to each row of a keyboard matrix and reading the columns for key actuation is called scanning. The scan time is the time taken by the processor to scan all the rows one by one starting from first row and coming back to the first row again.

62. What are the tasks involved in keyboard interface?

The tasks involved in keyboard interfacing are sensing a key actuation, debouncing the key and generating key codes (Decoding the key). These tasks are performed by software if the keyboard is interfaced through ports and they are performed by hardware if the keyboard is interfaced through 8279.

63. How a keyboard matrix is formed in keyboard interface using 8279?

The return lines, RLo to RL7 of 8279 are used to form the columns of keyboard matrix. In decoded scan the scan lines SLo to SL3 of 8279 are used to form the rows of keyboard matrix. In encoded scan mode, the output lines of external decoder are used as rows of keyboard matrix.

64. What is scanning in display and what is the scan time?

In display devices, the process of sending display codes to 7 –segment LEDs to display the LEDs one by one is called scanning (or multiplexed display). The scan time is the time taken to display all the 7-segment LEDs one by one, starting from first LED and coming back to the first LED again.

65. What is meant by 2-key lockout and N-key rollover?

2-Key Lockout: When two keys are pressed simultaneously, one key pressed first will be recognized and code will be generated.
N-Key Rollover: When a key is pressed continuously, the same key will be recognized several times, after each debounce.

66. List the functions performed by 8279.

a. Keyboard scanning.
b. Keyboard debouncing.
c. Keycode generation.
d. Intimating key pressing to CPU through Interrupt.
e. Storing display codes.
f. Output display codes to LED/LCDs.
g. Display refreshing.
ADC / DAC:

67. What are the different types of ADC?

The different types of ADC are successive approximation ADC, counter type ADC flash type ADC, integrator converters and voltage-to-frequency converters
.
68. What is settling or conversion time in DAC?
The time taken by the DAC to convert a given digital data to corresponding analog signal is called conversion time.

69. What is most commonly employed circuit in DAC?

The most commonly employed circuit in DAC is R/2R ladder network.

70. What are the internal devices of typical DAC?

The internal devices of DAC are R/2R ladder network, an internal latch and Current to Voltage converting amplifier.

71. What is the significance of address bus A0, A1 & A2 in ADC?

The analog input voltage may be taken for conversion into digital output from eight input channels. A particular input channel is selected by providing appropriate signals in the three address buses, A0, A1 & A2.

SERIAL COMMUNICATION STANDARDS:

72. How the RS -232C serial bus is interfaced to TTL logic device?

The RS-232C signal voltage levels are not compatible with TTL logic levels. Hence for interfacing TTL devices to RS-232C serial bus, level converters are used. The popularly used level converters are MC 1488 & MC 1489 or MAX 232.

73. What is RS-232C Standard?

The RS232C is a serial bus consisting of a maximum of 25 signals, which are standardized by EIA (Electronic Industry Association). The first 9 signals are sufficient for most of the serial data transmission.

74. What is the voltage level used in RS232C standard?

The voltage levels are
Logic LOW (0) : –3V to –15V
Logic HIGH (1) : +3V to +15V
Commonly used voltage levels are +12V (logic HIGH) and –12V (logic LOW).

75. What is the importance of Level converters?

The RS-232C signal levels are not compatible with TTL logic levels. Hence for interfacing TTL devices, level converters or RS-232C line drivers are employed. The popularly used level converters are
• MCI488 - TTL to RS232C level converter
• MCI489 - RS232C to TTL level converter
• MAX 232 - Bi-directional level converter.
(Max 232 is equivalent to a combination of MC1488 and MC1489 in single IC)

76. What are two important lines in I2C Standard?

The I2C bus uses a bi-directional Serial Clock Line [SCL] and Serial Data Lines [SDA]. Both lines are pulled high via a resistor [Rp]. Due to its two-wire nature (one clock, one data), it provides only half-duplex communication.

77. What are the modes of data rate in I2C standard?

Three speed modes are specified: Standard; 100kbps [Bits per Second], Fast mode; 400kbps,

High speed mode 3.4Mbps.

78. What is BPIB?

GPIB stands for General Purpose Interface Bus. It is communication standard developed by Hewlett Packard, for parallel data transfer between computers and instruments. Its IEEE standard number is IEEE 488.1. It supports data rate of 1 Mbps with upto maximum of 15 devices.

79. What are the modes in which 8086 can operate?

The 8086 can operate in two modes and they are minimum (or uniprocessor) mode and maximum (or multiprocessor) mode.

80. What are the hardware interrupts of 8086?

The interrupts of 8085 are INTR and NMI. The INTR is general maskable interruput and NMI is non-maskable interrupt.

81 How clock signal is generated in 8086? What is the maximum internal clock frequency of 8086?

The 8086 does not have on-chip clock generation circuit. Hence the clock generator chip, 8284 is connected to the CLK pin of8086. The clock signal supplied by 8284 is divided by three for internal use. The maximum internal clock frequency of8086 is 5MHz.

82. What is pipelined architecture?

In pipelined architecture the processor will have number of functional units and the execution time of functional units is overlapped. Each functional unit works independently most of the time.

83. What are the functional units available in 8086 architecture?

The bus interface unit (BIU) and execution unit (EU) are the two functional units available in 8086 processor.

84. List the segment registers of 8086.

The segment registers of 8086 are, Code segment (CS), Data segment (DS), Stack segment (SS)
and Extra segment (ES) registers.

85. What is the difference between segment register and general purpose register?

The segment registers are used to store 16 bit segment base address of the four memory segments. The general purpose registers are used as the source or destination register during data transfer and computation, as pointers to memory and as counters.

86. What is queue? How queue is implemented in 8086?

A data structure which can be accessed on the basis of first in first out is called queue. The 8086 has six numbers of 8-bit FIFO registers, which is used for instruction queue.

87. Write the special functions carried by the general purpose registers of 8086.

The special functions carried by the registers of 8086 are the following.
Register Special function
AX 16-bit Accumulator
AL 8-bit Accumulator
BX Base Register
CX Count Register
DX Data Register

88. Write the flags of 8086.

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
- - - - O D I T S Z - Ac - P - Cy
The 8086 has nine flags and they are
1. Carry Flag (CF) 6. Overflow Flag (OF)
2. Parity Flag (PF) 7. Trace Flag (TF)
3. Auxiliary carry Flag (AF) 8. Interrupt Flag (IF)
4. Zero Flag (ZF) 9. Direction Flag (DF)
5. Sign Flag (SF)

89. What are processor control bits?

The flags TF, IF and DF of 8086 are used to control the processor operation and so they are called control bits.

90. Describe the difference between the instructions MOV AX, 2437H and MOV AX,[2437H].

91Difference between the instructions MOV AX, 2437H and MOV AX,[2437H] are former instruction takes 2437 as 16-bit data and latter instruction takes 2437 as 16-bit address.

92. State the function of Direction flag in 8086.

Direction flag is used with string instructions. If DF= 0, the string is processed from its beginning with the first element having the lowest address. Otherwise, the string is processed from the high address towards the low address.

93. What happens in 8086 processor, when

a. overflow of sum occurs during addition of signed numbers. (Ans: Ov Flag is Set)
b. overflow of quotient occurs during division operation. (Ans: type0-divide by zero interrupt is generated).

94. In 8086 processor the code segment contains 4000H and instruction pointer contains 9F20H. Find the memory location addressed by the processor.

Segment address 4000 - 0100 0000 0000 0000
Shifted to left by four bits - 0100 0000 0000 0000 0000
(+) Offset address - 1001 1111 0010 0000

Physical address - - 0100 1001 1111 0010 0000 = 49F20H

\The Calculated Physical address = 49F20H

95. Discuss the functions of the following prefixes: LOCK, ESCAPE

LOCK :
In a multiprocessor system each microprocessor has its own local buses and memory. The

individual microprocessors are connected together by a system bus so that each can access system resources such as disk drives or memory. Each microprocessor only takes control of the system bus when it needs to access some system resources.
The LOCK prefix allows a microprocessor to make sure that another processor does not take control of the system bus while it is in the middle of a critical instruction which uses the system bus.
ESCAPE:
This instruction is used to pass instructions to a coprocessor such as the 8087 math coprocessor which shares the address and data bus with an 8086.

96. What are the flag manipulation instructions of 8086?

LAHF : Load AH from low byte of flag register.
SAHF : Store AH to low byte of flag register
PUSHF : Push content of flag to the stack.
POPF : Pop content of stack and load it in the flag register.

97 .Give the contents of the flag register after execution of following addition.
0110 0101 1101 0001
+ 0010 0011 0101 1001

1000 1001 0010 1010

SF = 1, ZF = 0, PF = 1, CF = 0, AF = 0, OF=1.

98. What are the three groups of signals in 8086?

The 8086 signals are categorized in three groups. They are :
i. The signals having common function in minimum and maximum mode.
ii. The signals having special functions for minimum mode,
iii. The signals having special functions for maximum mode.

99. What are the uses of AD0 – AD15 lines?

These are the time multiplexed memory 15 address and data lines. Address remains on the line during T I state ,while data is available on the data bus during T2, T3, TW and T4. Here T1, T2, T3, T4 and Tw are the clock states of a machine cycle. Tw is a wait state. These lines are active high and float to a tristate during interrupt acknowledge and local bus hold acknowledge cycles.

100. What is the operation of RD signal?

Read signal RD when low, indicates the peripherals that the processor is performing a memory (or) I/O read operation.